

WHAT IS CLAIMED IS:

1. A multi-mode voltage-controlled oscillator (VCO) comprising:
 2. a ring oscillator circuit comprising a series connection of an odd number K of logic inverter gates, wherein K is greater than three;
 4. a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward conduction circuit coupled in parallel with a selected sequence of logic inverter gates within said K logic inverter gates; and
 7. a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, wherein a frequency range of said multi-mode VCO is selected in response to states of said first and second mode control signals.
1. The multi-mode VCO of claim 1, wherein said selectable inverter circuit comprises:
 3. a selectable logic inverter gate having an input coupled to said first inverter input, an output coupled to said first inverter output, a first terminal for receiving a first power supply voltage, and a second terminal for receiving a second power supply voltage;
 6. a first electronic switch having a first control input receiving said first mode control signal, a first switch terminal receiving said first power supply voltage, and a second switch terminal coupled to said first terminal of said selectable inverter; and
 9. a second electronic switch having a second control input receiving said second mode signal, a third switch terminal receiving said second power supply voltage, and a fourth switch terminal coupled to said second terminal of said selectable inverter.

1 3. The multi-mode VCO of claim 1, wherein said forward conduction circuit
2 comprises:

3 a control inverter having a second input and a second output; and
4 a bi-directional conduction circuit having a third input, a third output, a first
5 control input, and a second control input, said second input coupled to said first input, said
6 second output coupled to said third input, said third output coupled to said first output,
7 said first control input coupled to a first control voltage, and said second control input
8 coupled to a second control voltage.

1 4. The multi-mode VCO of claim 3, wherein said bi-directional conduction circuit
2 comprises:

3 a first P channel metal oxide semiconductor (PFET) having a first drain terminal,
4 a first source terminal and a first gate terminal; and

5 a first NFET having a second drain terminal, a second source terminal and a
6 second gate terminal, wherein said first drain terminal and said second drain terminal are
7 coupled to said third input, said first source terminal and said second source terminal are
8 coupled to said third output, said first gate terminal is coupled to said first control input,
9 and said second gate terminal is coupled to said second control input.

1 5. The multi-mode VCO of claim 2, wherein said first electronic switch comprises
2 a third PFET having a fifth drain terminal, a fifth source terminal and a fifth gate terminal,
3 said fifth source terminal coupled to said first electronic switch terminal, said fifth drain
4 terminal coupled to said second electronic switch terminal, and said fifth gate terminal
5 coupled to said first control input.

1 6. The multi-mode VCO of claim 2, wherein said second electronic switch comprises
2 a third NFET having a sixth drain terminal, a sixth source terminal and a sixth gate
3 terminal, said sixth source terminal coupled to said third electronic switch terminal, said
4 sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth gate
5 terminal coupled to said second control input.

1 7. The multi-mode VCO of claim 1, wherein said selected sequence from said K
2 logic inverter gates comprises a series of three inverter logic gates.

1 8. The multi-mode VCO of claim 1, wherein each of said K inverter logic gates of
2 said ring oscillator are coupled in parallel with a corresponding one of said selectable
3 inverter circuits.

1 9. A data processing system comprising:

2 a central processor unit (CPU), operable to generate a clock signal with a phase
3 lock loop (PLL) clock generator, having a ring oscillator circuit configured as a series
4 connection of an odd number K of logic inverter gates, wherein K is greater than three,
5 a forward conduction circuit having a first input, a first output, and receiving control
6 inputs, said forward conduction circuit coupled in parallel with a selected sequence from
7 said K logic inverter gates, and a selectable inverter circuit, having a first inverter input,
8 a first inverter output and receiving a first mode control signal and a second mode control
9 signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and
10 said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth
11 logic inverter gate selected from said K logic inverter gates;]

12 a random access memory (RAM);

13 a read only memory (ROM);

14 an I/O adapter; and

15 a bus system coupling said CPU to said ROM, said I/O adapter, and said RAM,
16 wherein a frequency range of said ring oscillator circuit is selected in response to states
17 of said first and second mode control signals.

1 10. The data processing system of claim 9, wherein said selectable inverter circuit
2 comprises:

3 a selectable logic inverter gate having an input coupled to said first inverter input,
4 an output coupled to said first inverter output, a first terminal for receiving a first power
5 supply voltage, and a second terminal for receiving a second power supply voltage;

6 a first electronic switch having a first control input receiving said first mode
7 control signal, a first switch terminal receiving said first power supply voltage, and a

8 second switch terminal coupled to said first terminal of said selectable inverter; and
9 a second electronic switch having a second control input receiving said second
10 mode signal, a third switch terminal receiving said second power supply voltage, and a
11 fourth switch terminal coupled to said second terminal of said selectable inverter.

1 11. The data processing system of claim 9, wherein said forward conduction circuit
2 comprises:

3 a control inverter having a second input and a second output; and
4 a bi-directional conduction circuit having a third input, a third output, a first
5 control input, and a second control input, said second input coupled to said first input, said
6 second output coupled to said third input, said third output coupled to said first output,
7 said first control input coupled to a first control voltage, and said second control input
8 coupled to a second control voltage.

1 12. The data processing system of claim 11, wherein said bi-directional conduction
2 circuit comprises:

3 a first P channel metal oxide semiconductor (PFET) having a first drain terminal,
4 a first source terminal and a first gate terminal; and
5 a first NFET having a second drain terminal, a second source terminal and a
6 second gate terminal, wherein said first drain terminal and said second drain terminal are
7 coupled to said third input, said first source terminal and said second source terminal are
8 coupled to said third output, said first gate terminal is coupled to said first control input,
9 and said second gate terminal is coupled to said second control input.

1 13. The data processing system of claim 10, wherein said first electronic switch
2 comprises a third PFET having a fifth drain terminal, a fifth source terminal and a fifth

3 gate terminal, said fifth source terminal coupled to said first electronic switch terminal,
4 said fifth drain terminal coupled to said second electronic switch terminal, and said fifth
5 gate terminal coupled to said first control input.

1 14. The data processing system of claim 10, wherein said second electronic switch
2 comprises ~~a third NFET~~ having a sixth drain terminal, a sixth source terminal and a sixth
3 gate terminal, said sixth source terminal coupled to said third electronic switch terminal,
4 said sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth
5 gate terminal coupled to said second control input.

1 15. The data processing system of claim 9, wherein said selected sequence from said
2 K logic inverter gates comprises a series of three inverter logic gates ,

1 16. The data processing system of claim 9, wherein each of said K inverter logic gates
2 of said ring oscillator are coupled in parallel with a corresponding one of said selectable
3 inverter circuits.

1 17. A phase lock loop (PLL) circuit comprising:

2 a phase/frequency comparator receiving a reference clock signal and a feedback

3 clock signal and generating a first control signal and a second control signal;

4 a charge pump circuit receiving said first control signal and said second control

5 signal and generating a charge pump output on a first and second charge pump nodes;

6 a first capacitor and a second capacitor coupled to said first and said second charge

7 pump nodes, respectively;

8 a voltage controlled oscillator (VCO) having a ring oscillator circuit having a

9 series connection of an odd number K of logic inverter gates, wherein K is greater than

10 three;

11 a forward conduction circuit having a first input, a first output, and receiving said

12 charge pump output, said forward conduction circuit coupled in parallel with a selected

13 sequence of logic inverter gates within said K logic inverter gates, and a selectable

14 inverter circuit, having a first inverter input, a first inverter output and receiving a first

15 mode control signal and a second mode control signal, said first inverter input coupled to

16 a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic

17 output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K

18 logic inverter gates, wherein a frequency range of said VCO is selected in response to

19 states of said first and second mode control signals; and

20 a signal frequency divider receiving said VCO output signal and generating said

21 feedback clock signal, wherein a frequency of said VCO is controlled in response to said

22 charge pump output and said first and second mode control signals.

1 18. The PLL circuit of claim 19, wherein said selectable inverter circuit comprises:

2 a selectable logic inverter gate having an input coupled to said first inverter input,

3 an output coupled to said first inverter output, a first terminal for receiving a first power
4 supply voltage, and a second terminal for receiving a second power supply voltage;

5 a first electronic switch having a first control input receiving said first mode
6 control signal, a first switch terminal receiving said first power supply voltage, and a
7 second switch terminal coupled to said first terminal of said selectable inverter; and

8 a second electronic switch having a second control input receiving said second mode signal,
9 a third switch terminal receiving said second power supply voltage, and a
10 fourth switch terminal coupled to said second terminal of said selectable inverter.

1 19. The PLL circuit of claim 19, wherein said forward conduction circuit comprises:
2 a control inverter having a second input and a second output; and

3 a bi-directional conduction circuit having a third input, a third output, a first
4 control input, and a second control input, said second input coupled to said first input, said
5 second output coupled to said third input, said third output coupled to said first output,
6 said first control input coupled to a first control voltage, and said second control input
7 coupled to a second control voltage.

1 20. The PLL circuit of claim 21, wherein said bi-directional conduction circuit
2 comprises:

3 a first P channel metal oxide semiconductor (PFET) having a first drain terminal,
4 a first source terminal and a first gate terminal; and

5 a first NFET having a second drain terminal, a second source terminal and a
6 second gate terminal, wherein said first drain terminal and said second drain terminal are
7 coupled to said third input, said first source terminal and said second source terminal are
8 coupled to said third output, said first gate terminal is coupled to said first control input,
9 and said second gate terminal is coupled to said second control input.

1 21. The PLL circuit of claim 20, wherein said first electronic switch comprises a third
2 PFET having a fifth drain terminal, a fifth source terminal and a fifth gate terminal, said
3 fifth source terminal coupled to said first electronic switch terminal, said fifth drain
4 terminal coupled to said second electronic switch terminal, and said fifth gate terminal
5 coupled to said first control input.

1 22. The PLL circuit of claim 20, wherein said second electronic switch comprises a
2 third NFET having a sixth drain terminal, a sixth source terminal and a sixth gate
3 terminal, said sixth source terminal coupled to said third electronic switch terminal, said
4 sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth gate
5 terminal coupled to said second control input.

1 23. The PLL circuit of claim 19, wherein said selected sequence from said K logic
2 inverter gates comprises a series of three inverter logic gates.

1 24. The PLL circuit of claim 19, wherein each of said K inverter logic gates of said
2 ring oscillator are coupled in parallel with a corresponding one of said selectable inverter
3 circuits.